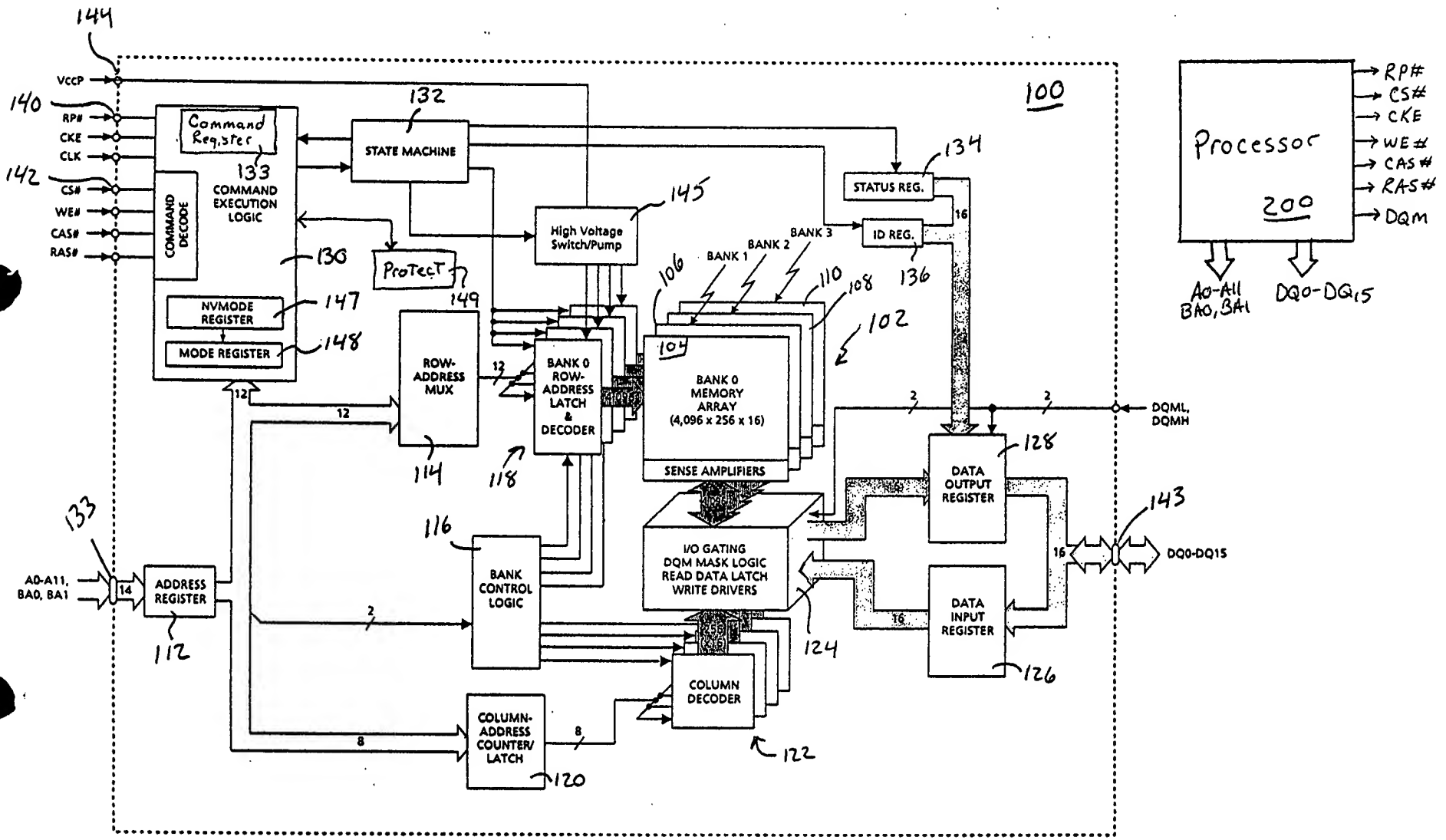


Fig. 1A

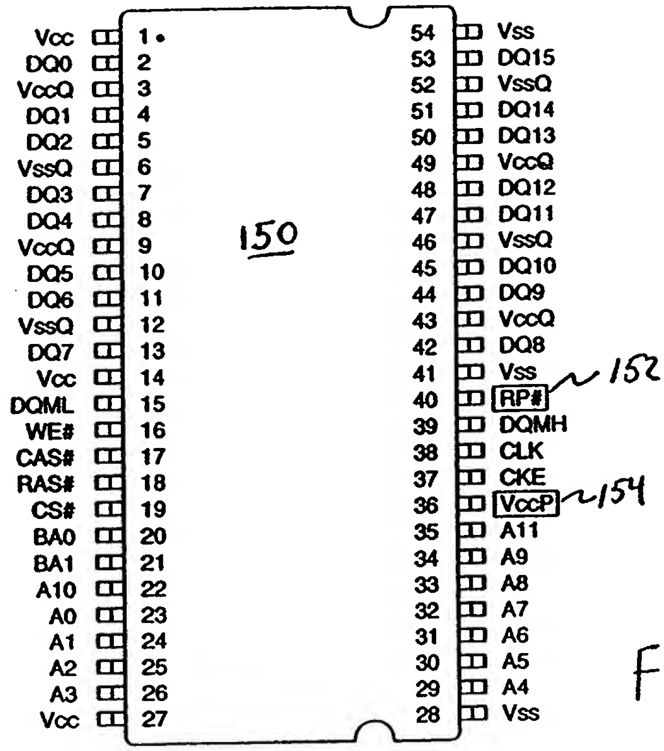


Fig. 1B

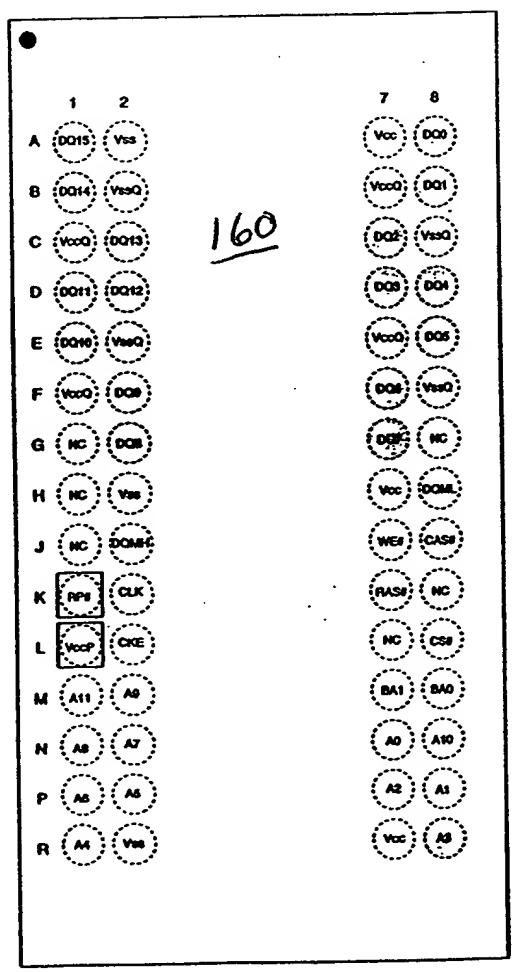


Fig. 1C

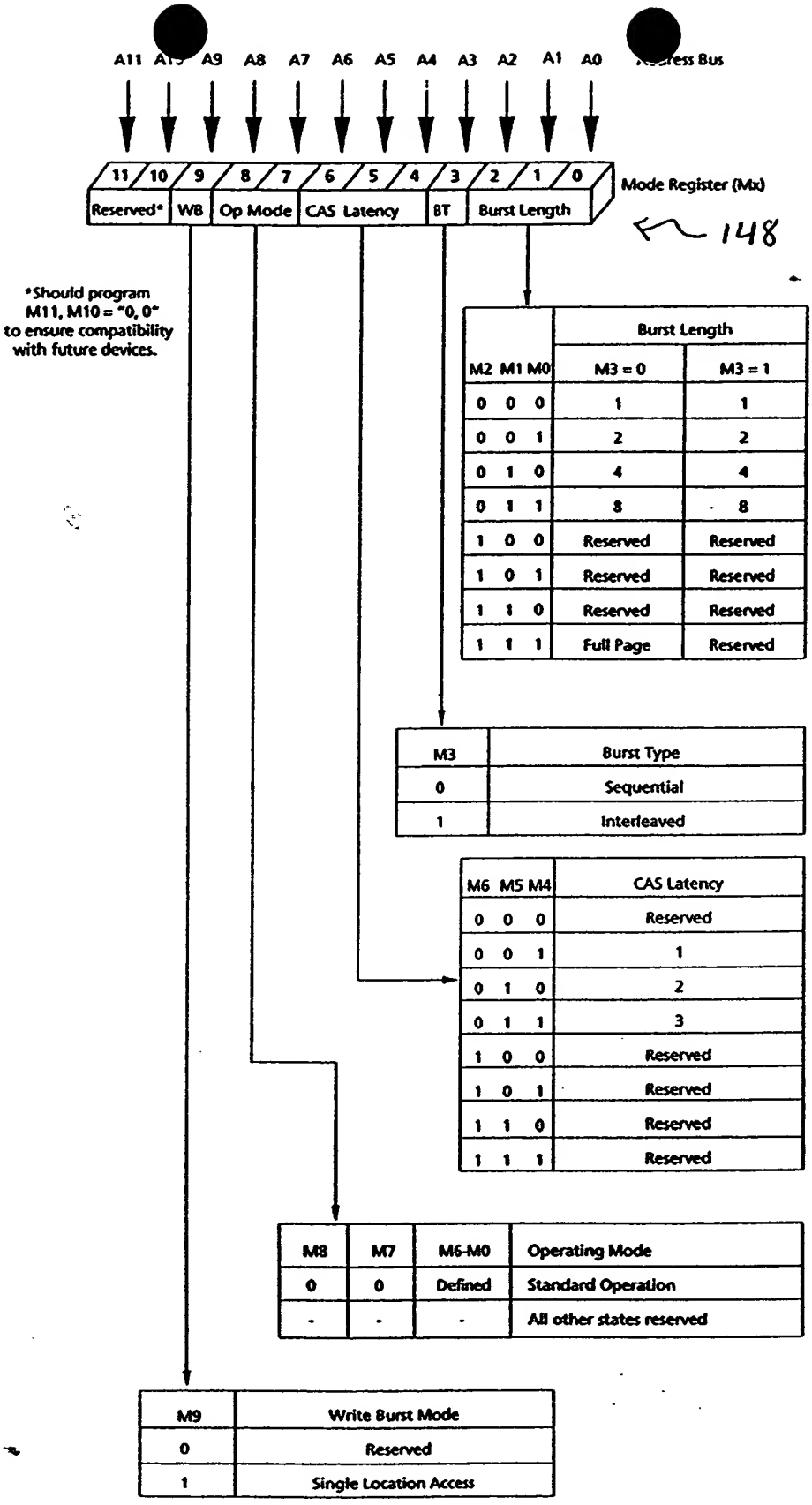

A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Address Bus
11 10 9 8 7 6 5 4 3 2 1 0
Reserved* WB Op Mode CAS Latency BT Burst Length
Mode Register (Mx)
148
*Should program M11, M10 = "0, 0" to ensure compatibility with future devices.
Burst Length
M2 M1 M0 | M3 = 0 | M3 = 1
0 0 0 | 1 | 1
0 0 1 | 2 | 2
0 1 0 | 4 | 4
0 1 1 | 8 | 8
1 0 0 | Reserved | Reserved
1 0 1 | Reserved | Reserved
1 1 0 | Reserved | Reserved
1 1 1 | Full Page | Reserved
M3 | Burst Type
0 | Sequential
1 | Interleaved
M6 M5 M4 | CAS Latency
0 0 0 | Reserved
0 0 1 | 1
0 1 0 | 2
0 1 1 | 3
1 0 0 | Reserved
1 0 1 | Reserved
1 1 0 | Reserved
1 1 1 | Reserved
M8 | M7 | M6-M0 | Operating Mode
0 | 0 | Defined | Standard Operation
- | - | - | All other states reserved
M9 | Write Burst Mode
0 | Reserved
1 | Single Location Access

Fig. 2

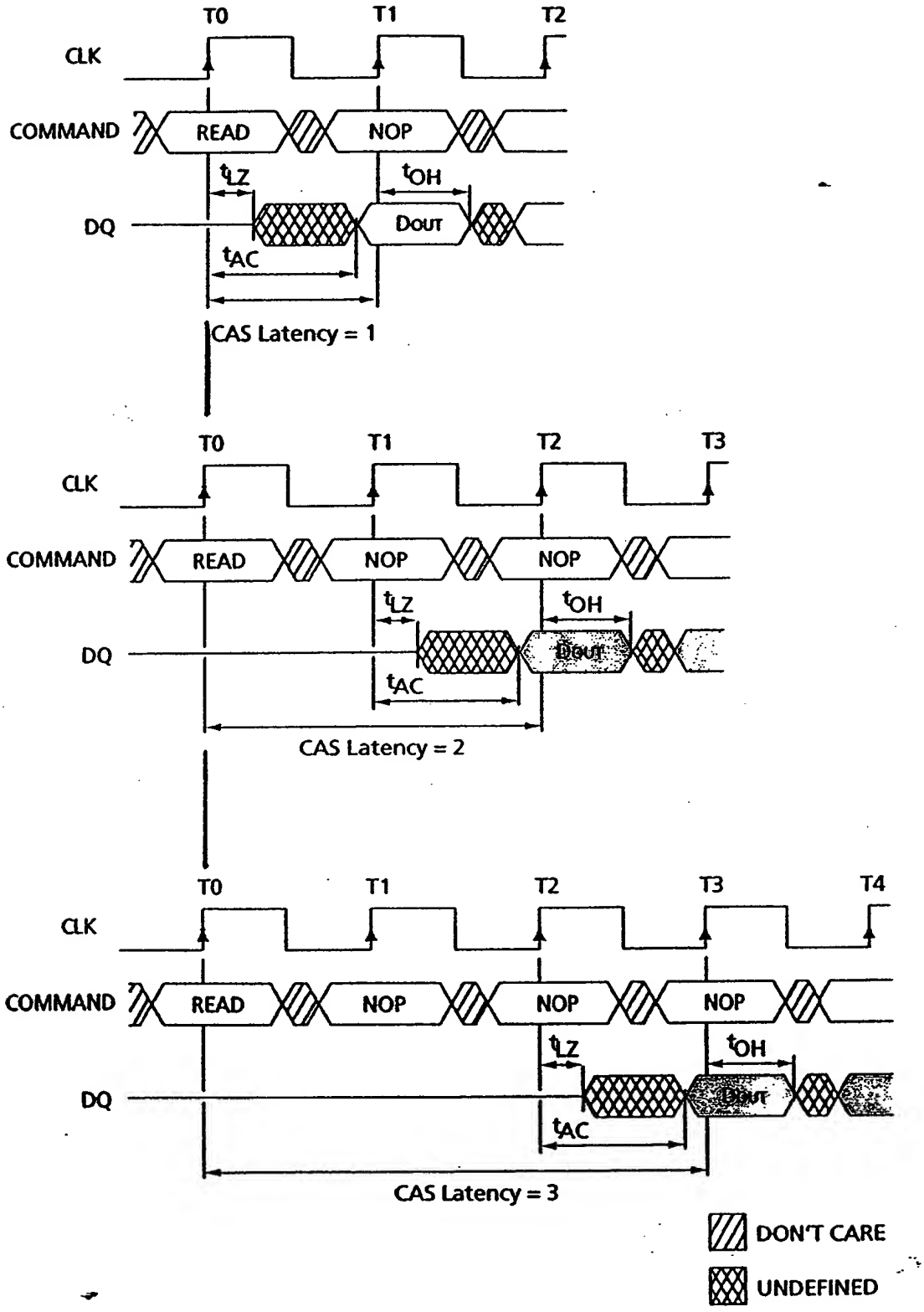

T0
T1
T2
CLK
COMMAND
READ
NOP
tLZ
tOH
DQ
DOUT
tAC
CAS Latency = 1
T0
T1
T2
T3
CLK
COMMAND
READ
NOP
NOP
tLZ
tOH
DQ
DOUT
tAC
CAS Latency = 2
T0
T1
T2
T3
T4
CLK
COMMAND
READ
NOP
NOP
NOP
tLZ
tOH
DQ
DOUT
tAC
CAS Latency = 3
DON'T CARE
UNDEFINED

Fig. 3

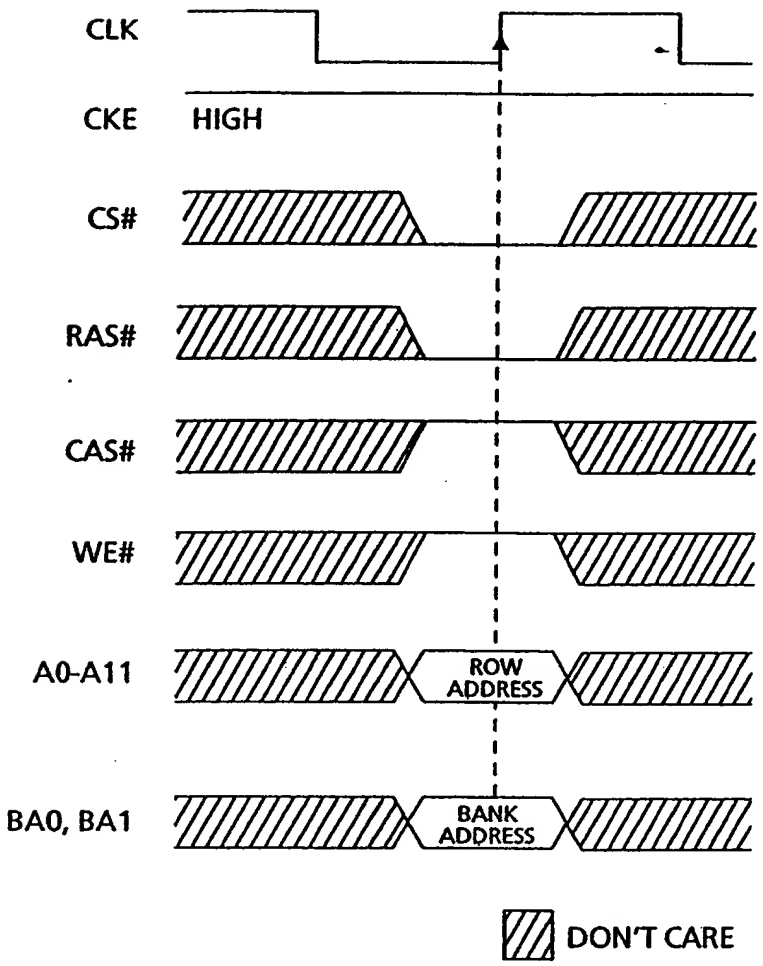


Fig. 4

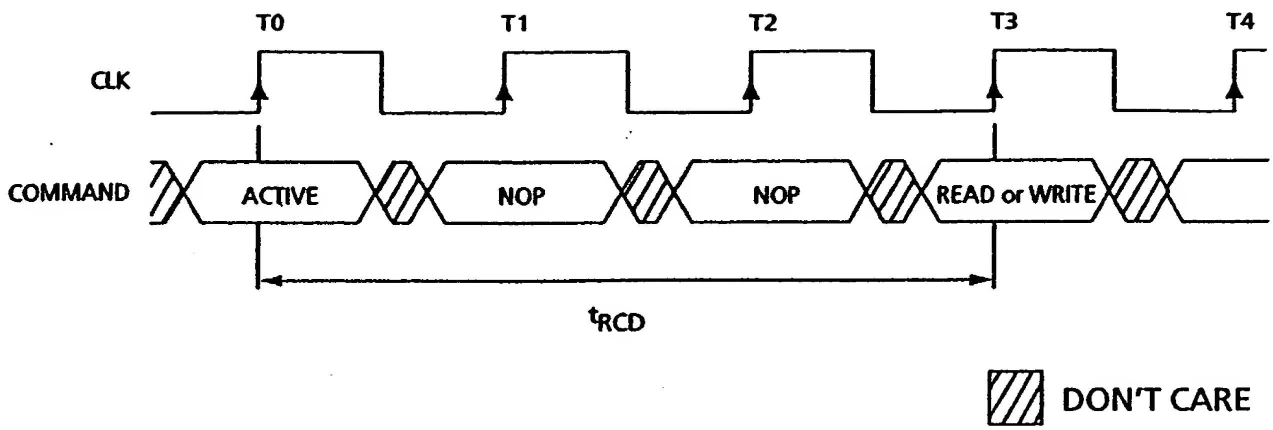


Fig. 5

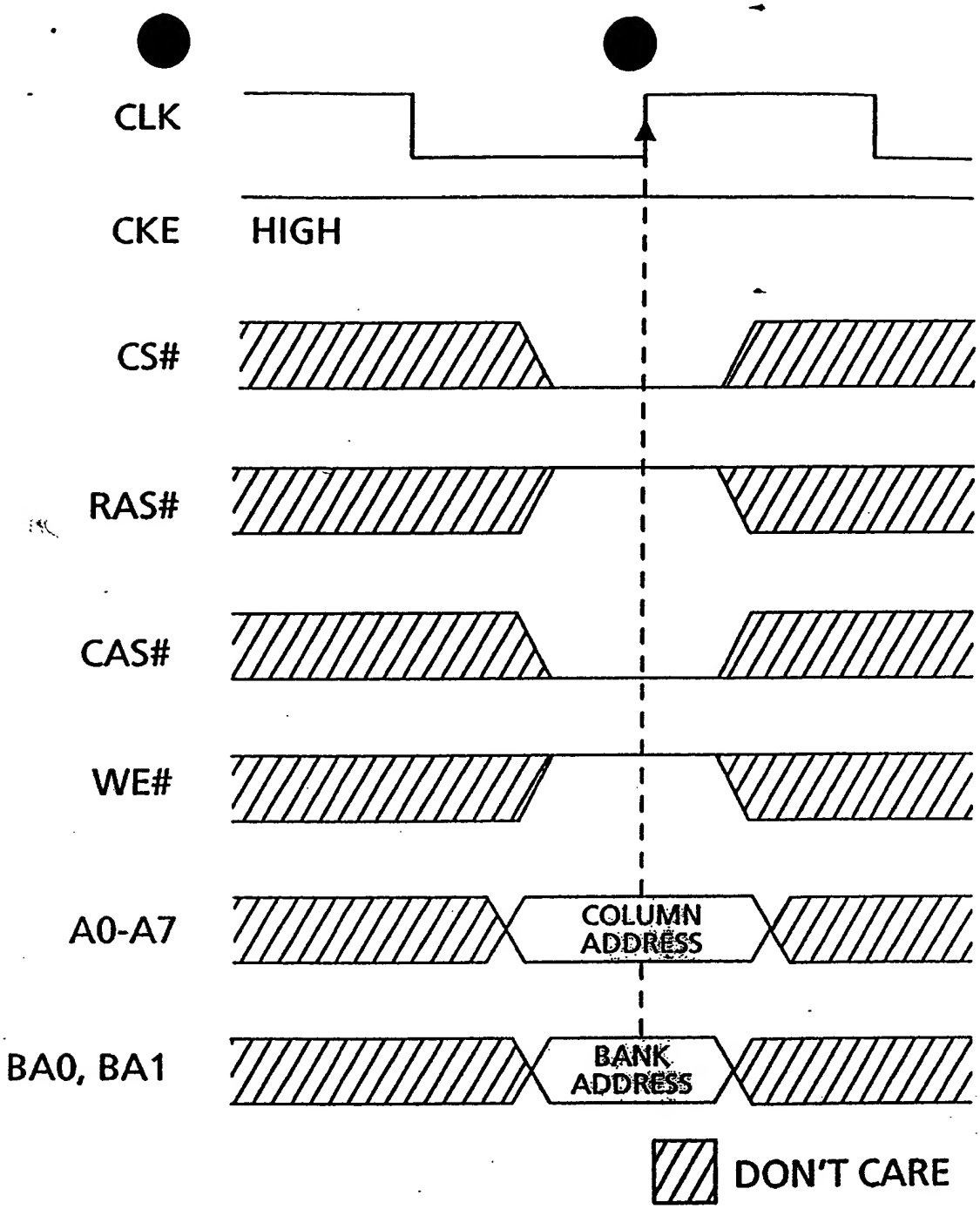
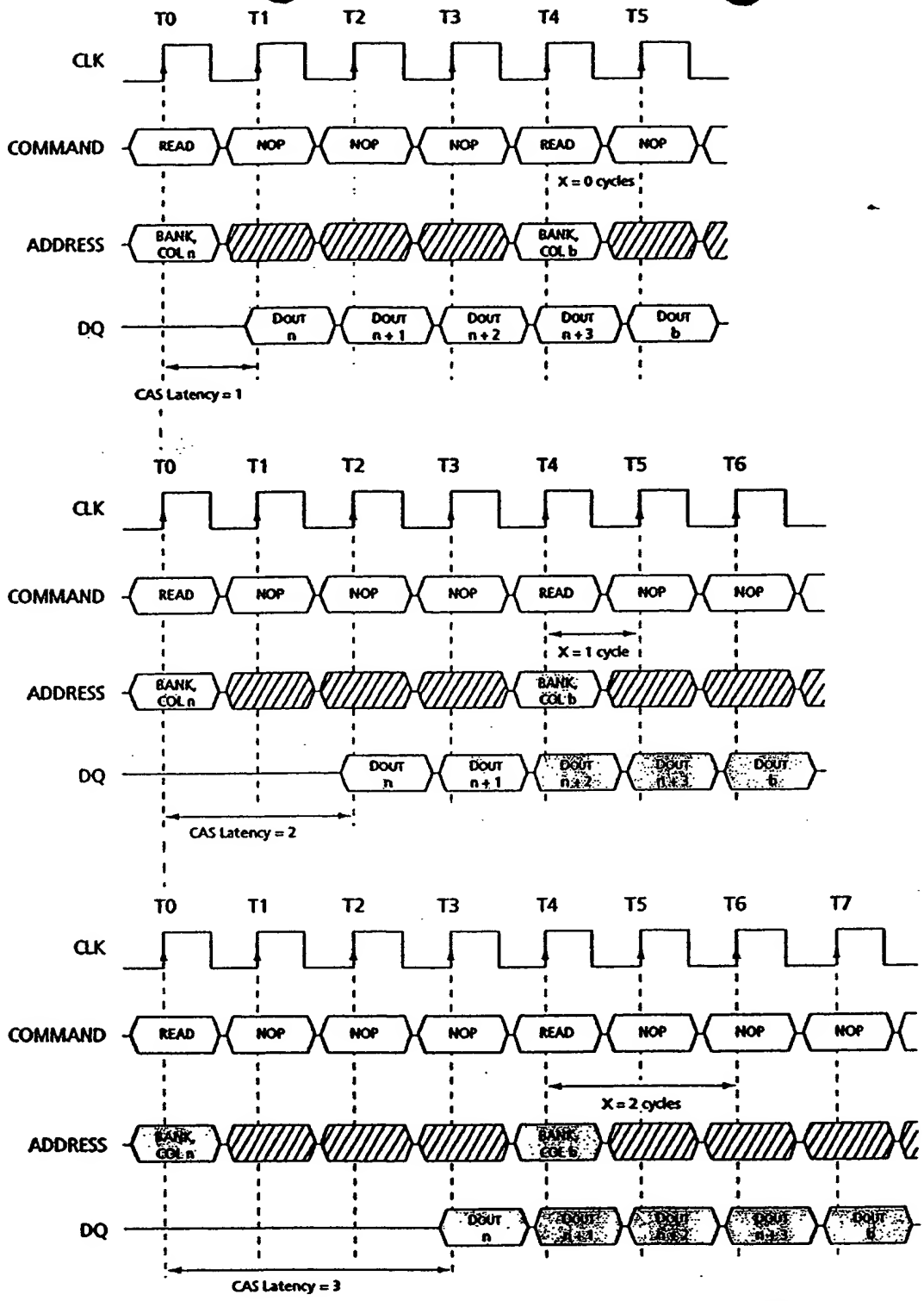
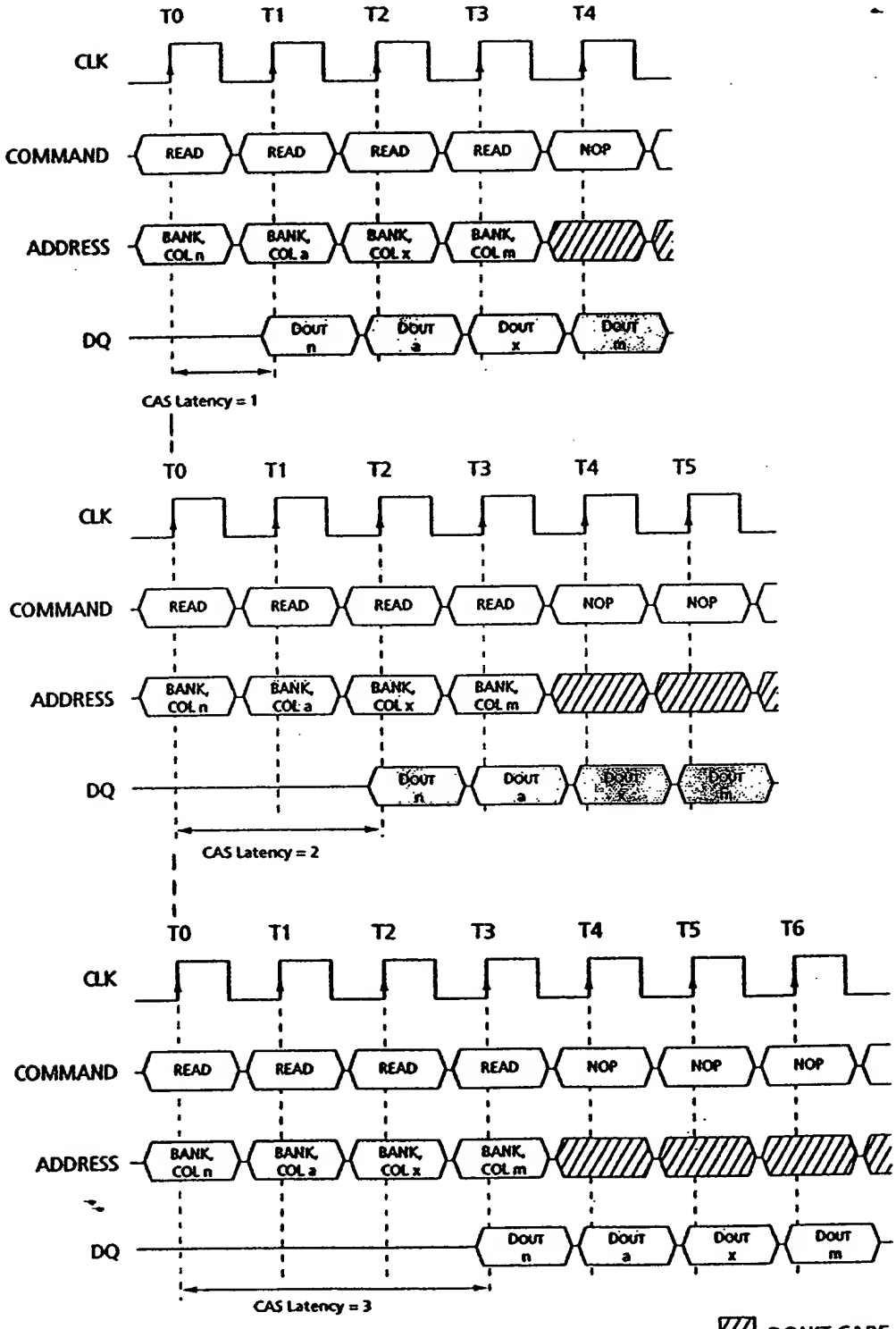

CLK
CKE
HIGH
CS#
RAS#
CAS#
WE#
A0-A7
COLUMN ADDRESS
BA0, BA1
BANK ADDRESS
DON'T CARE

Fig. 6



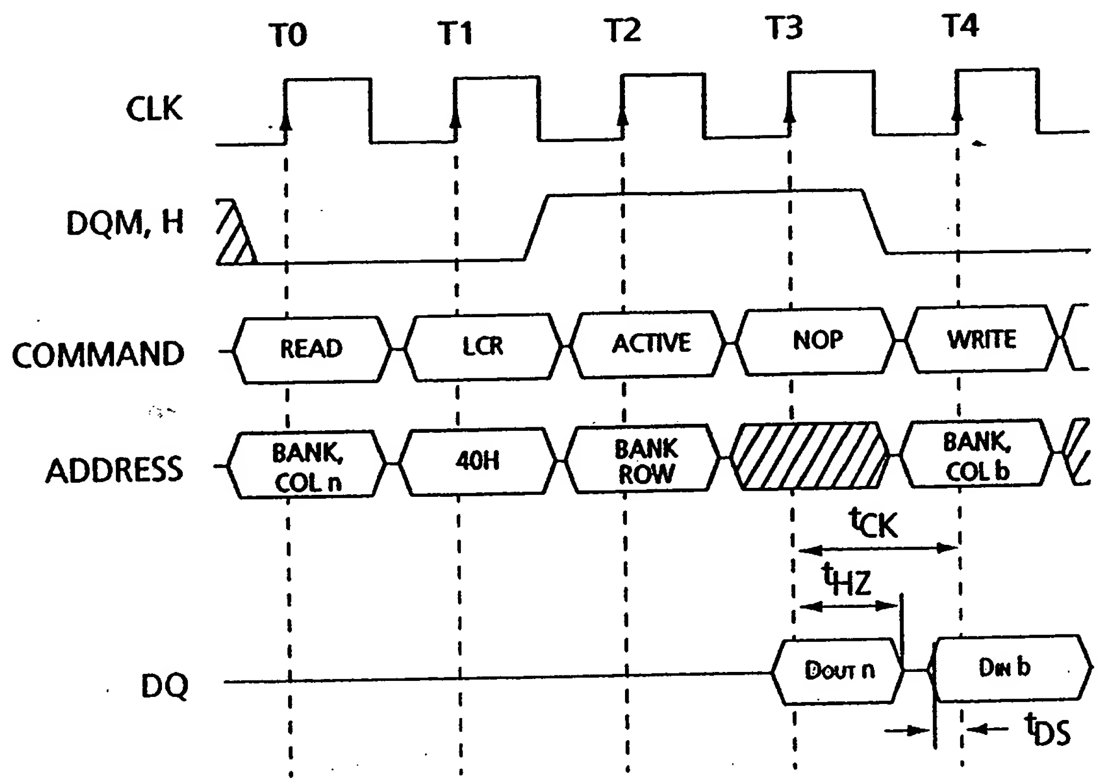
NOTE: Each READ command may be to either bank. DQM is LOW.

Fig. 7



NOTE: Each READ command may be to either bank. DQM is LOW.

Fig. 8



NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank. If a CAS latency of one is used, then DQM is not required.

DON'T CARE

Fig 9

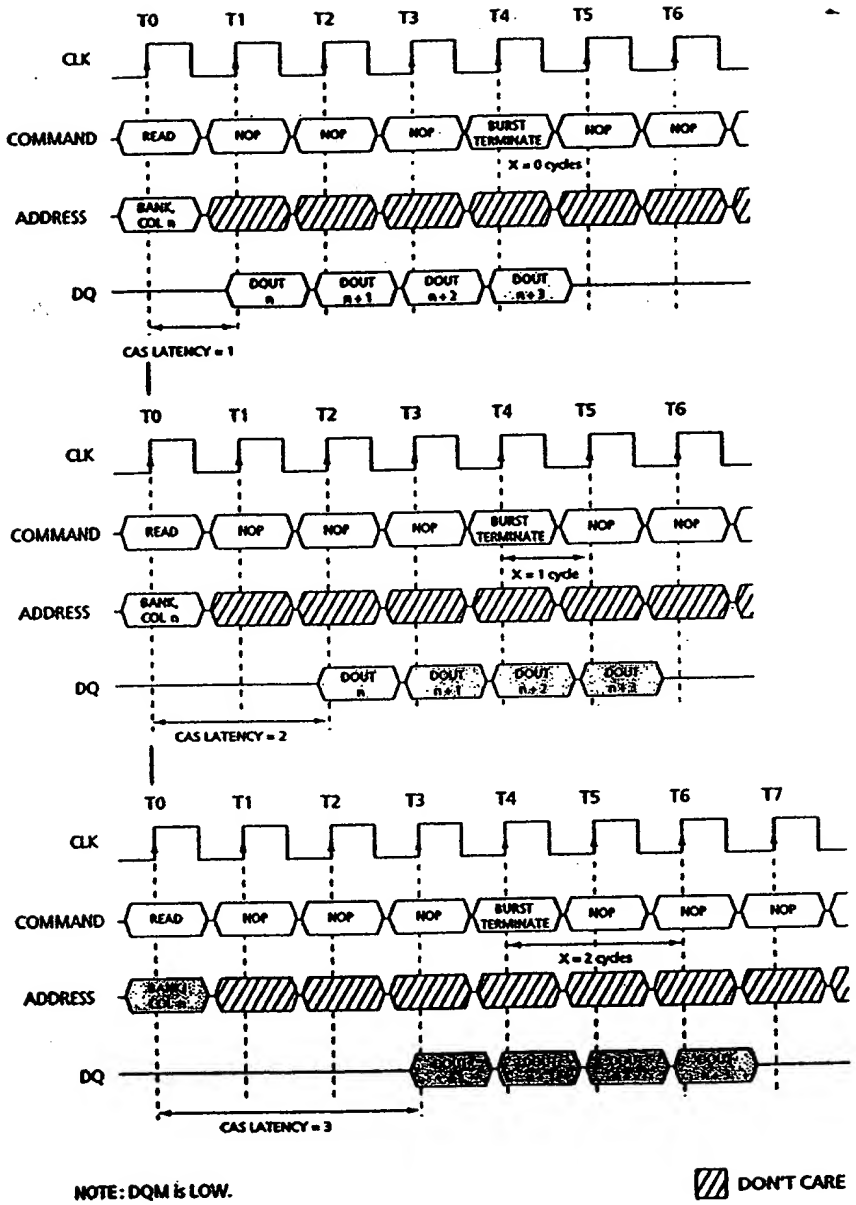

T0
T1
T2
T3
T4
T5
T6
CLK
COMMAND
READ
NOP
BURST TERMINATE
X = 0 cycles
ADDRESS
BANK, COL n
DQ
DOUT n
DOUT n+1
DOUT n+2
DOUT n+3
CAS LATENCY = 1
X = 1 cycle
CAS LATENCY = 2
T7
X = 2 cycles
CAS LATENCY = 3
NOTE: DQM is LOW.
DON'T CARE

Fig. 10

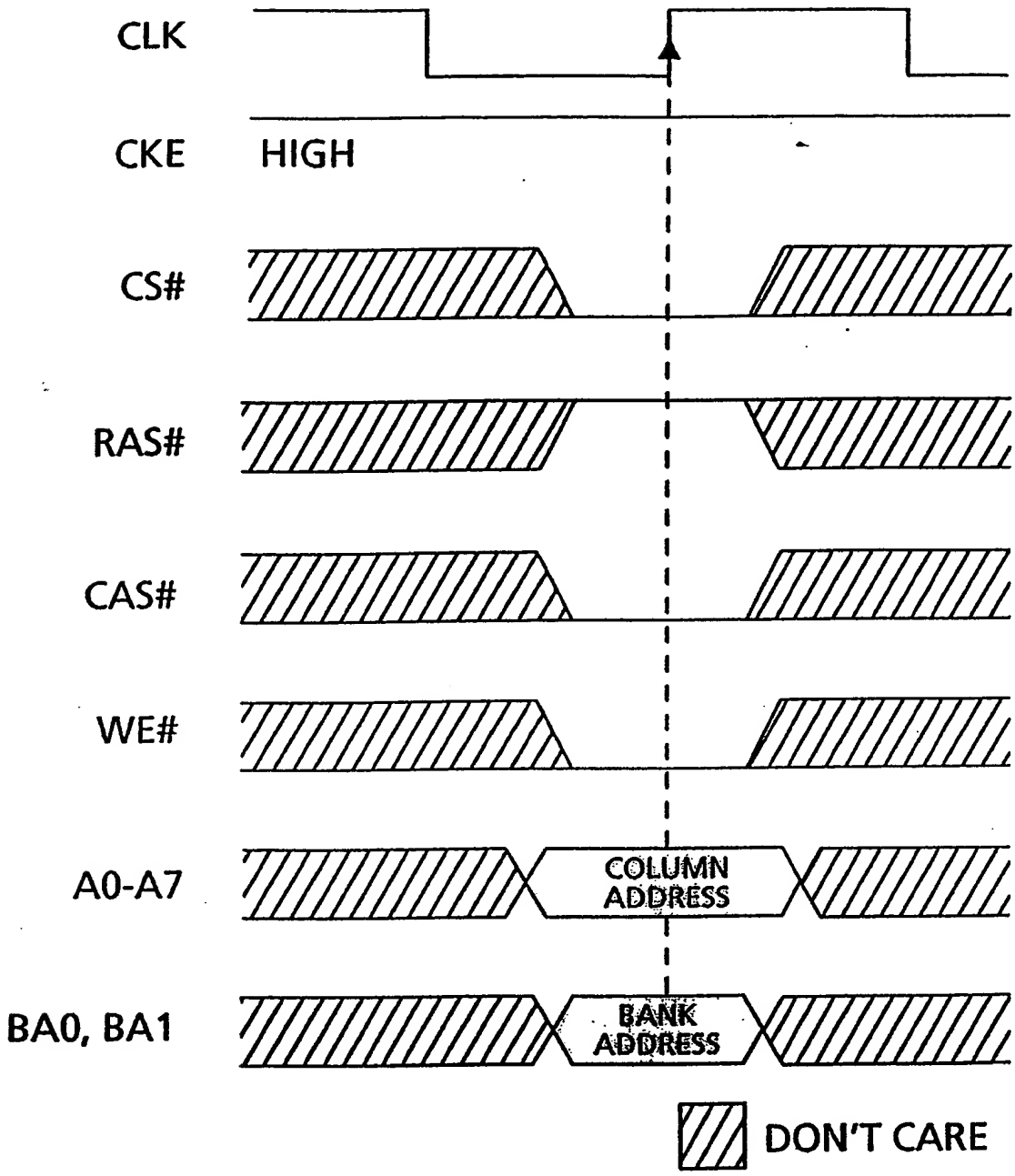
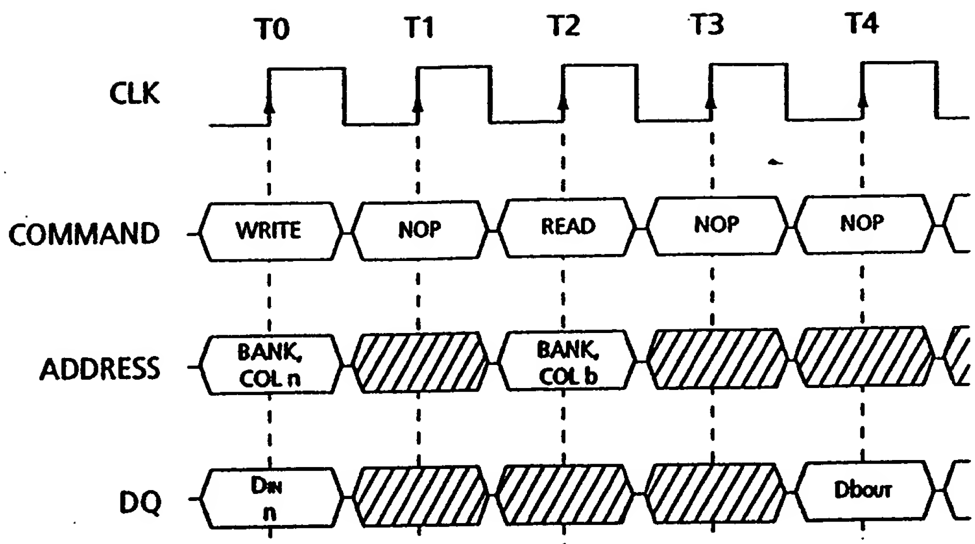

CLK
CKE
HIGH
CS#
RAS#
CAS#
WE#
A0-A7
COLUMN ADDRESS
BA0, BA1
BANK ADDRESS
DON'T CARE

Fig. 11



NOTE: A CAS latency of two is used for illustration. The WRITE command may be to any bank and the READ command may be to any bank. DQM is LOW. A READ to the bank undergoing the WRITE ISM operation may output invalid data. ... Tables 4 and 5.

DON'T CARE

Fig. 12

Coming out of a power-down sequence (active),
^{t}CKS (CKE setup time) must be greater than or equal to 3ns.

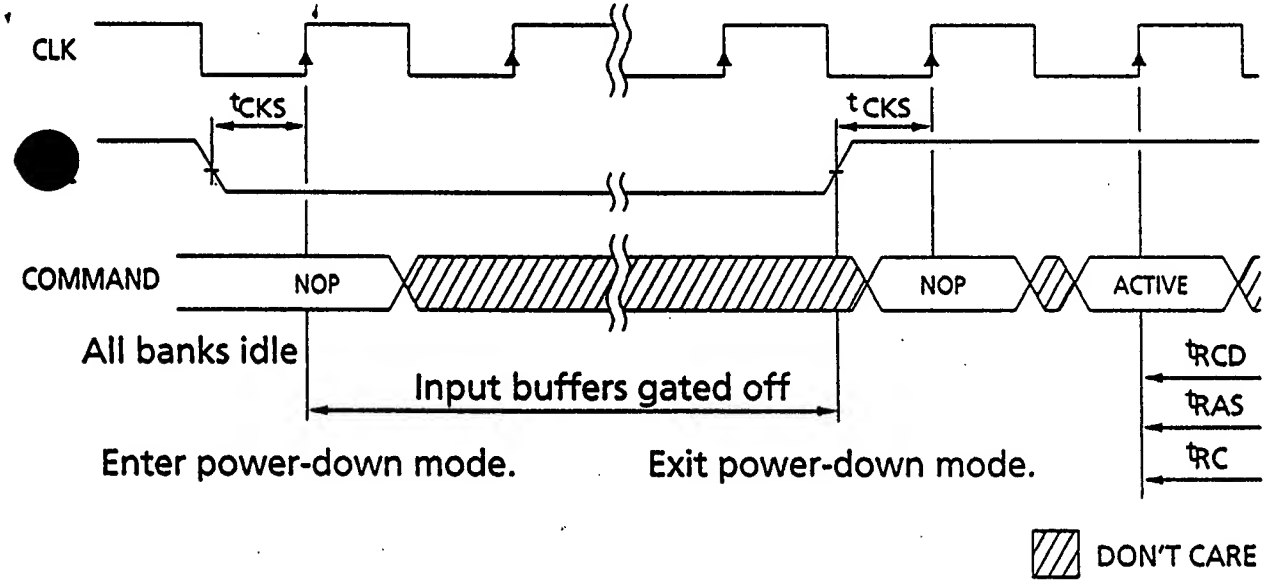
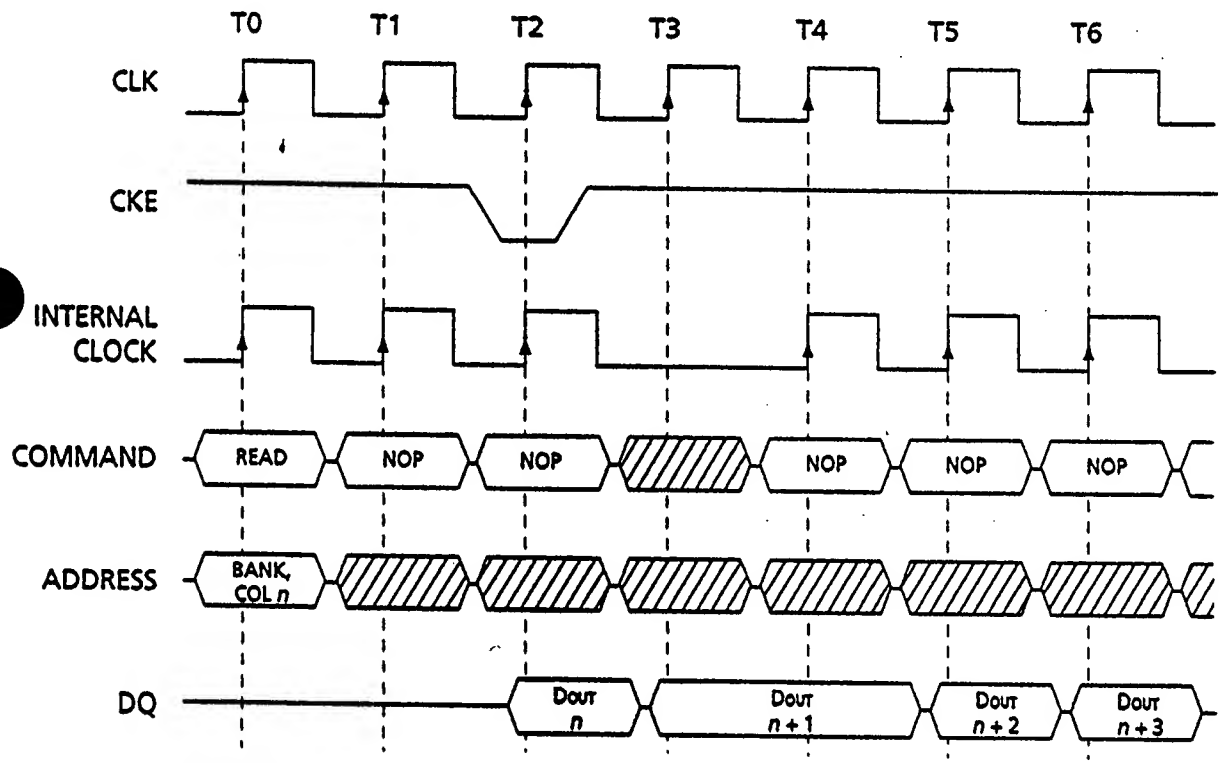


Fig. 13



NOTE: For this example, CAS latency = 2, burst length = 4 or greater, an DQM is LOW.

DON'T CARE

Fig. 14

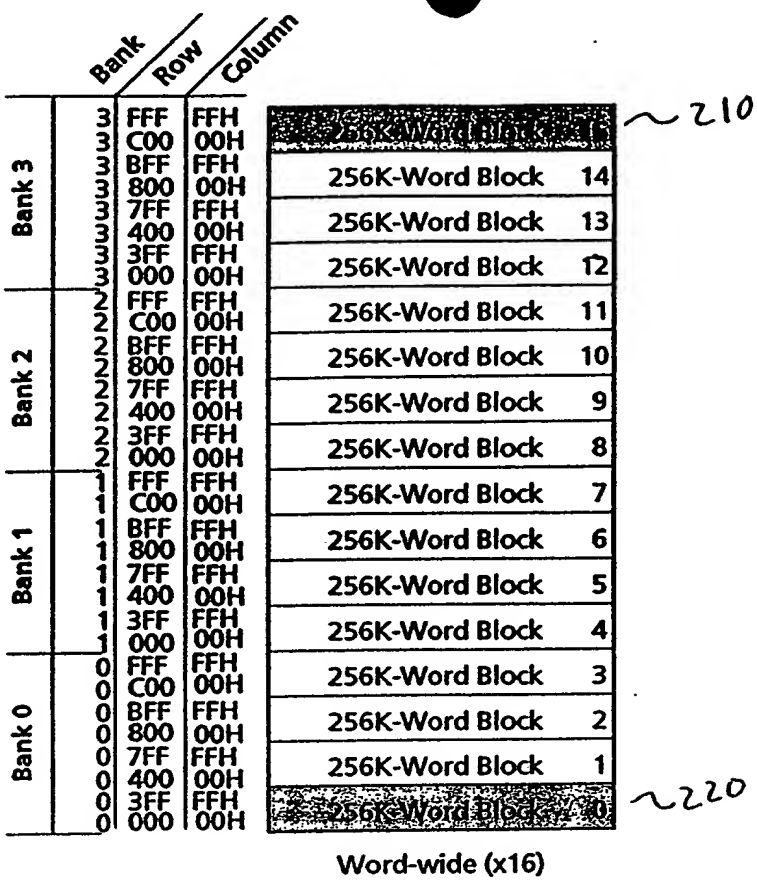


Fig. 15

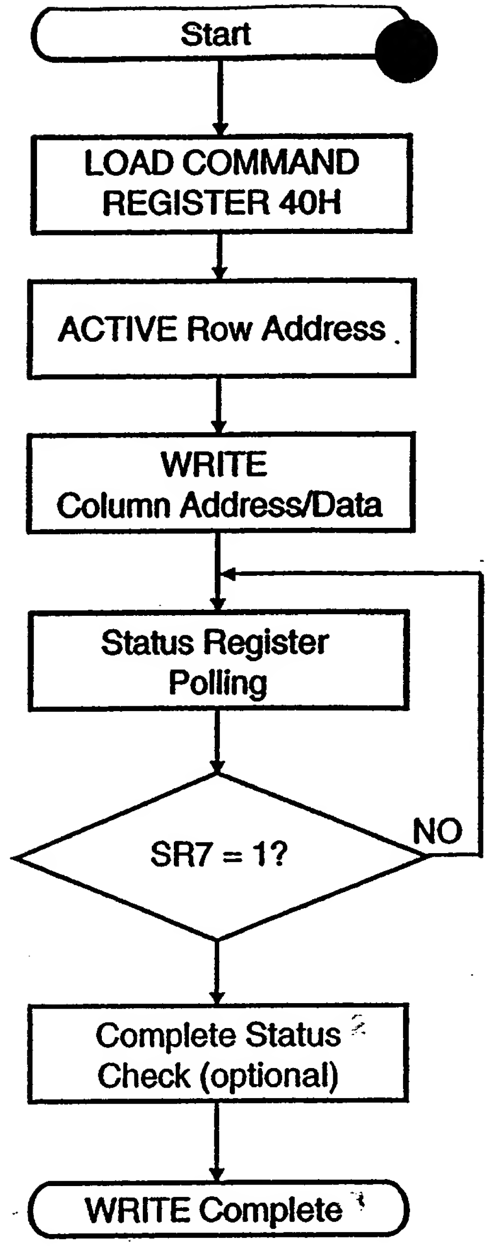


Fig. 16

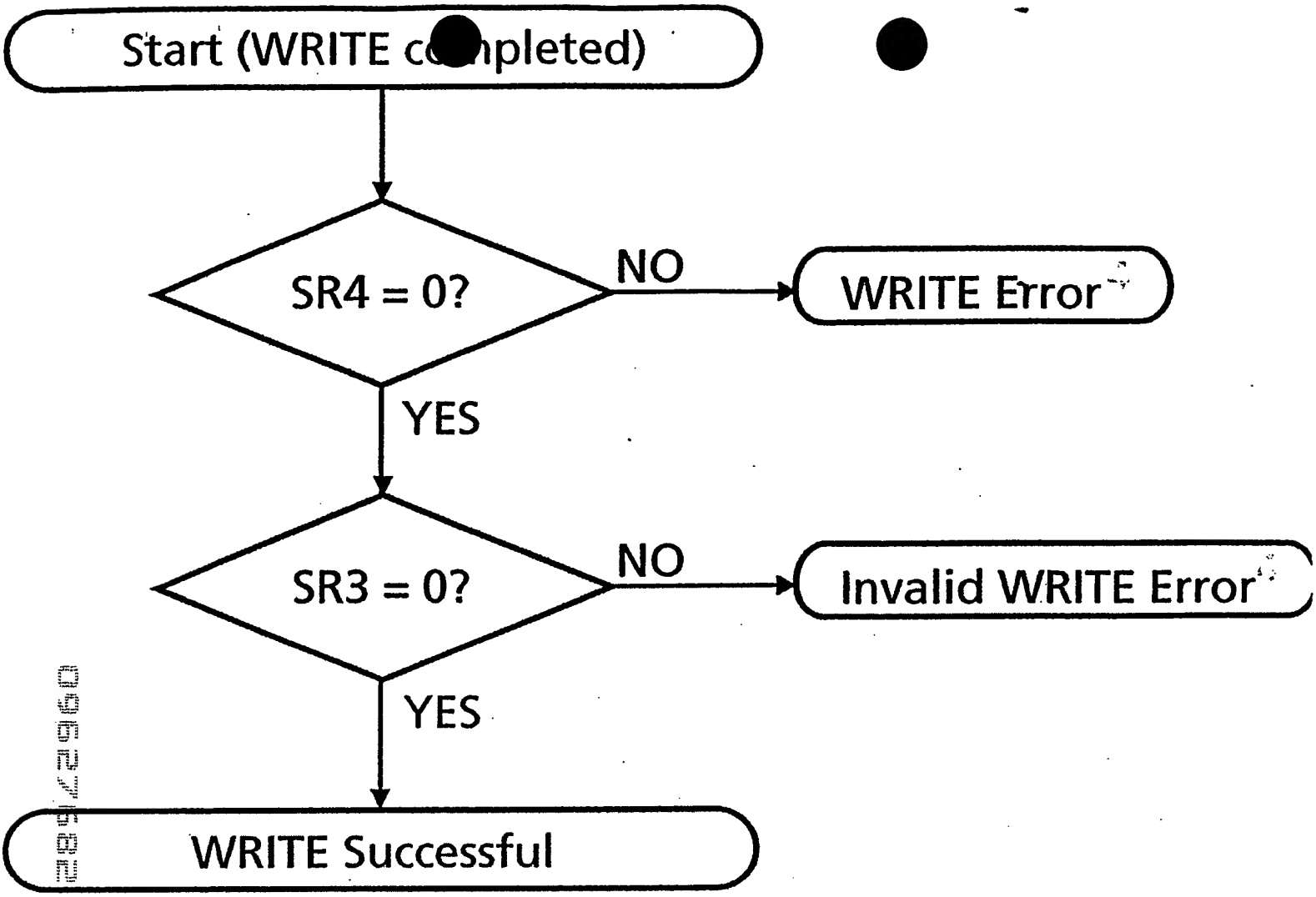

Start (WRITE completed)
SR4 = 0?
NO
WRITE Error
YES
SR3 = 0?
NO
Invalid WRITE Error
YES
WRITE Successful

Fig. 17

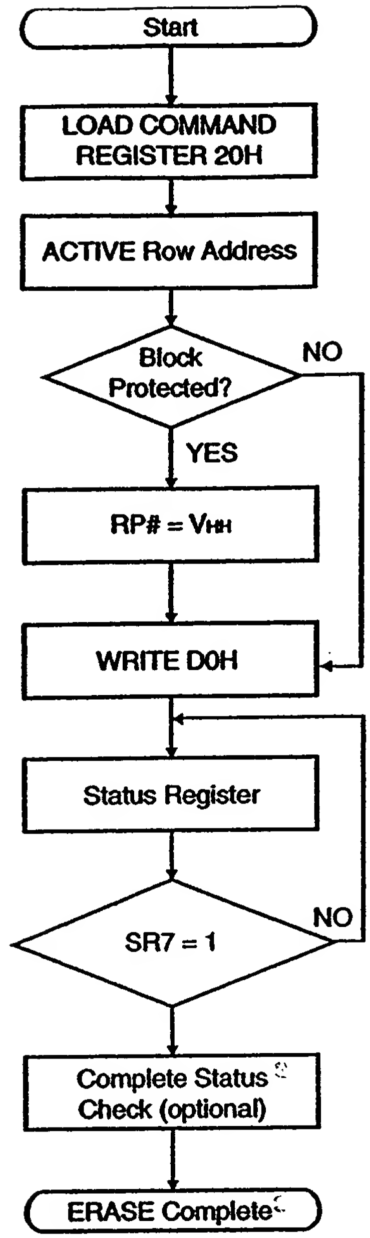


Fig. 18

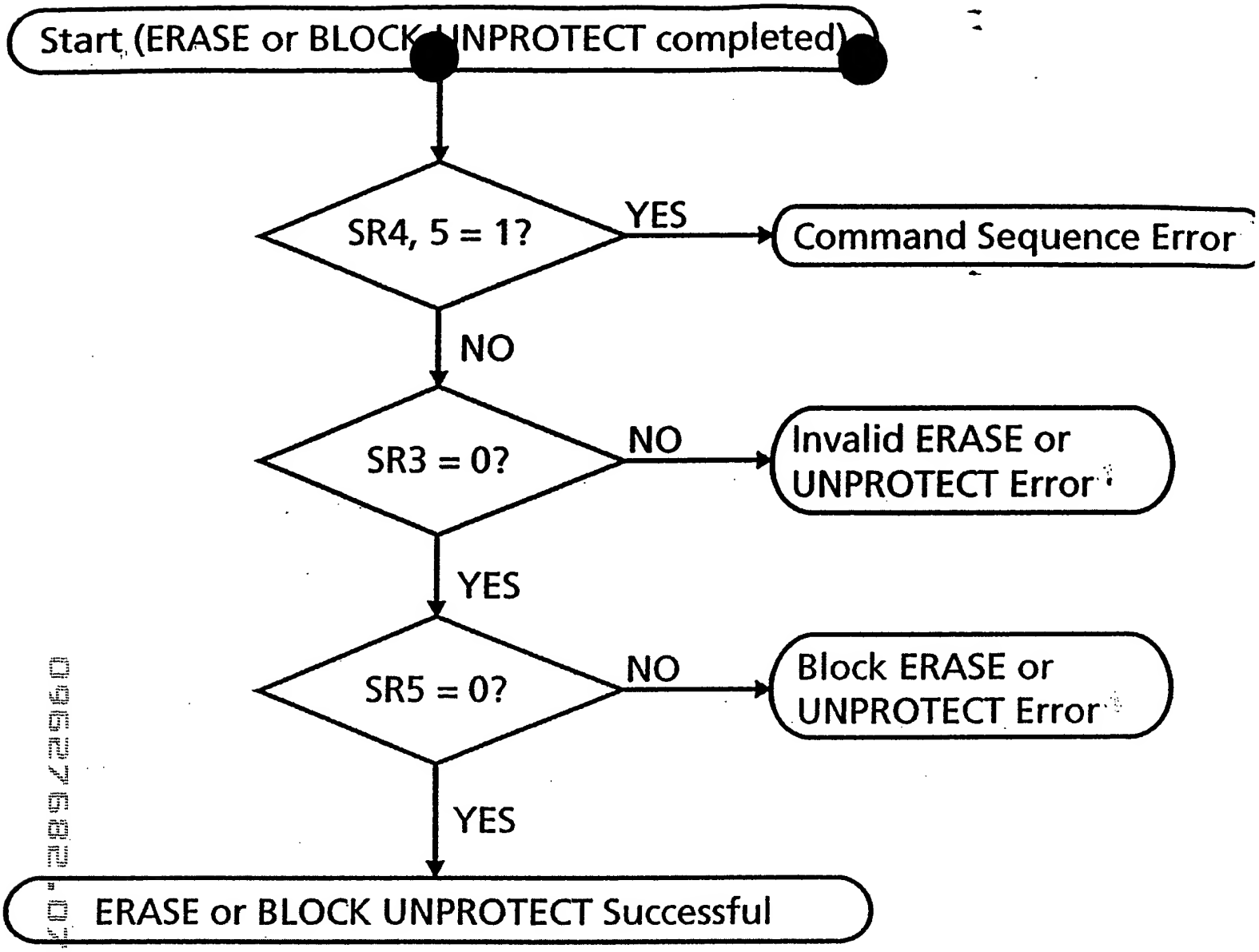

Start (ERASE or BLOCK UNPROTECT completed)
SR4, 5 = 1?
YES
Command Sequence Error
NO
SR3 = 0?
NO
Invalid ERASE or UNPROTECT Error
YES
SR5 = 0?
NO
Block ERASE or UNPROTECT Error
YES
ERASE or BLOCK UNPROTECT Successful

Fig. 19

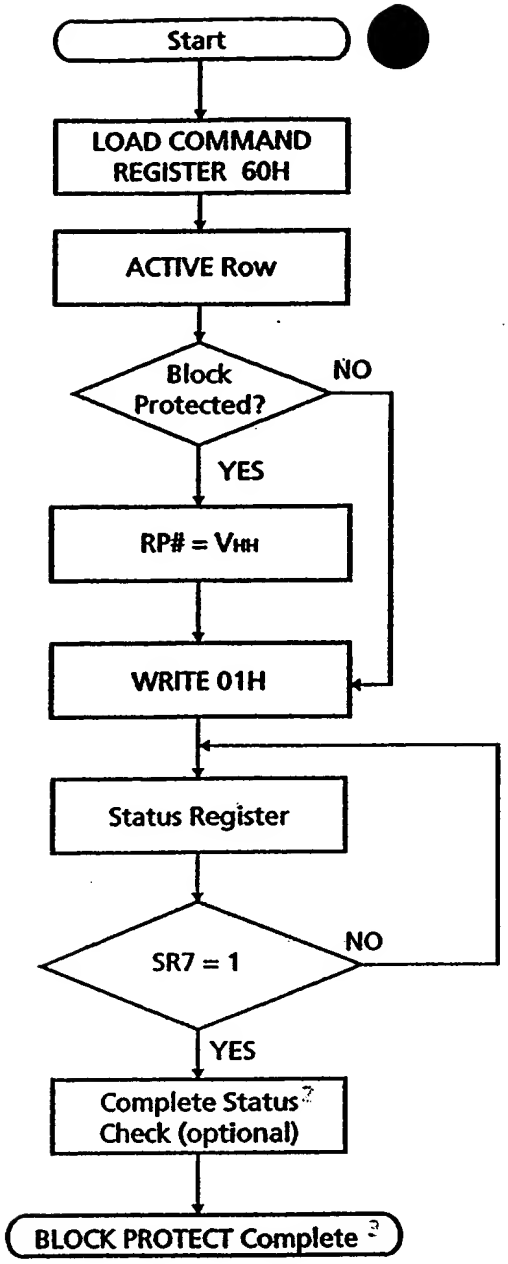

Start
LOAD COMMAND REGISTER 60H
ACTIVE Row
Block Protected?
NO
YES
RP# = VHH
WRITE 01H
Status Register
SR7 = 1
NO
YES
Complete Status Check (optional)
BLOCK PROTECT Complete

Fig. 20

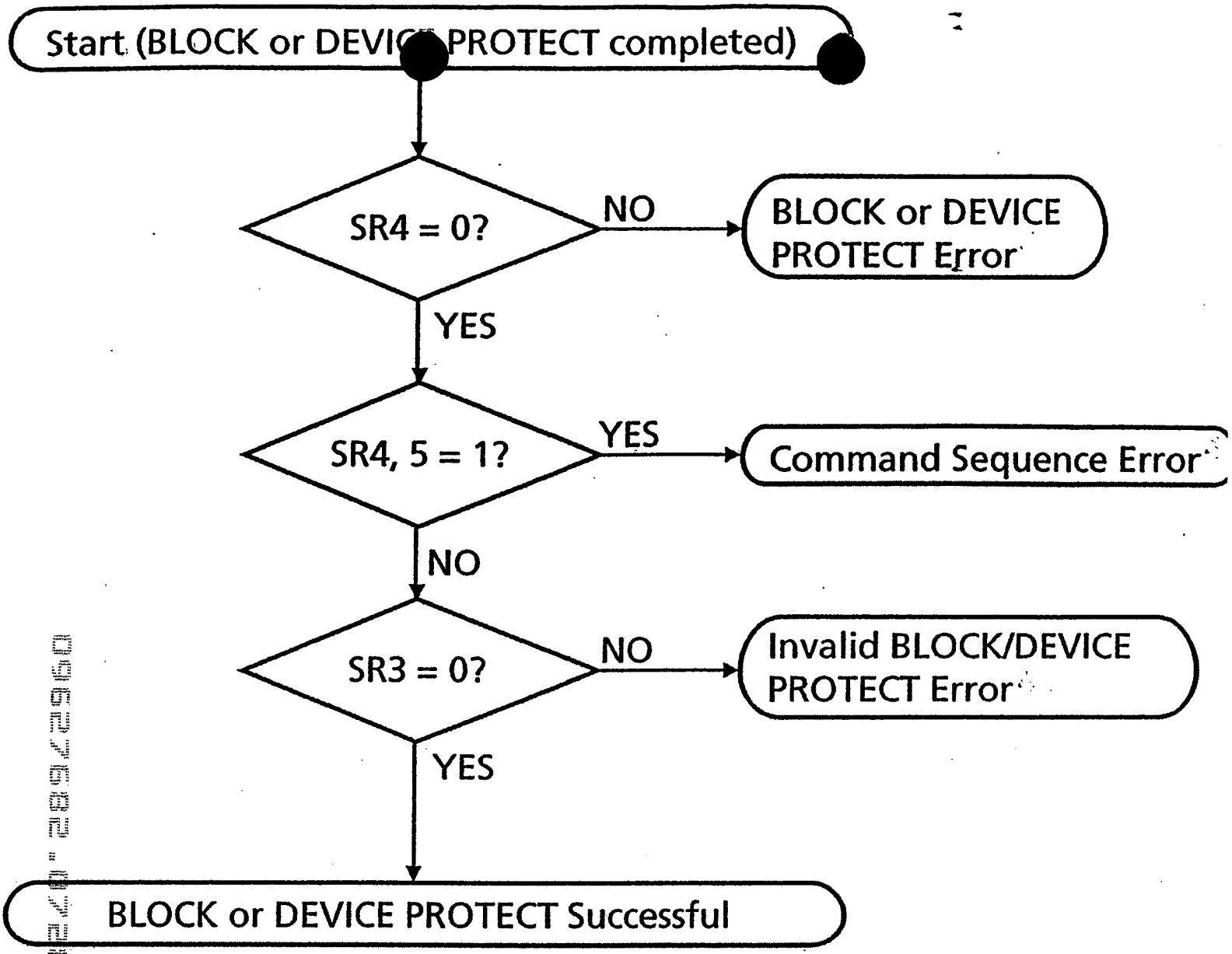

Start (BLOCK or DEVICE PROTECT completed)
SR4 = 0?
NO
BLOCK or DEVICE PROTECT Error
YES
SR4, 5 = 1?
YES
Command Sequence Error
NO
SR3 = 0?
NO
Invalid BLOCK/DEVICE PROTECT Error
YES
BLOCK or DEVICE PROTECT Successful

Fig. 21

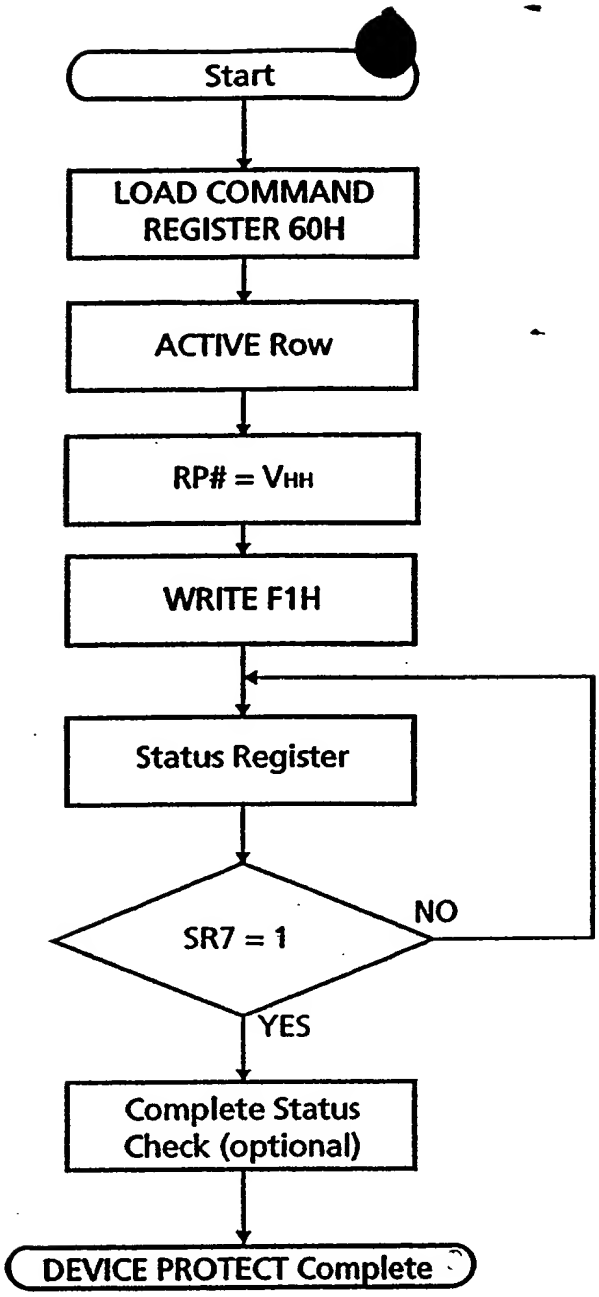

Start
LOAD COMMAND REGISTER 60H
ACTIVE Row
RP# = VHH
WRITE F1H
Status Register
SR7 = 1
NO
YES
Complete Status Check (optional)
DEVICE PROTECT Complete

Fig. 22

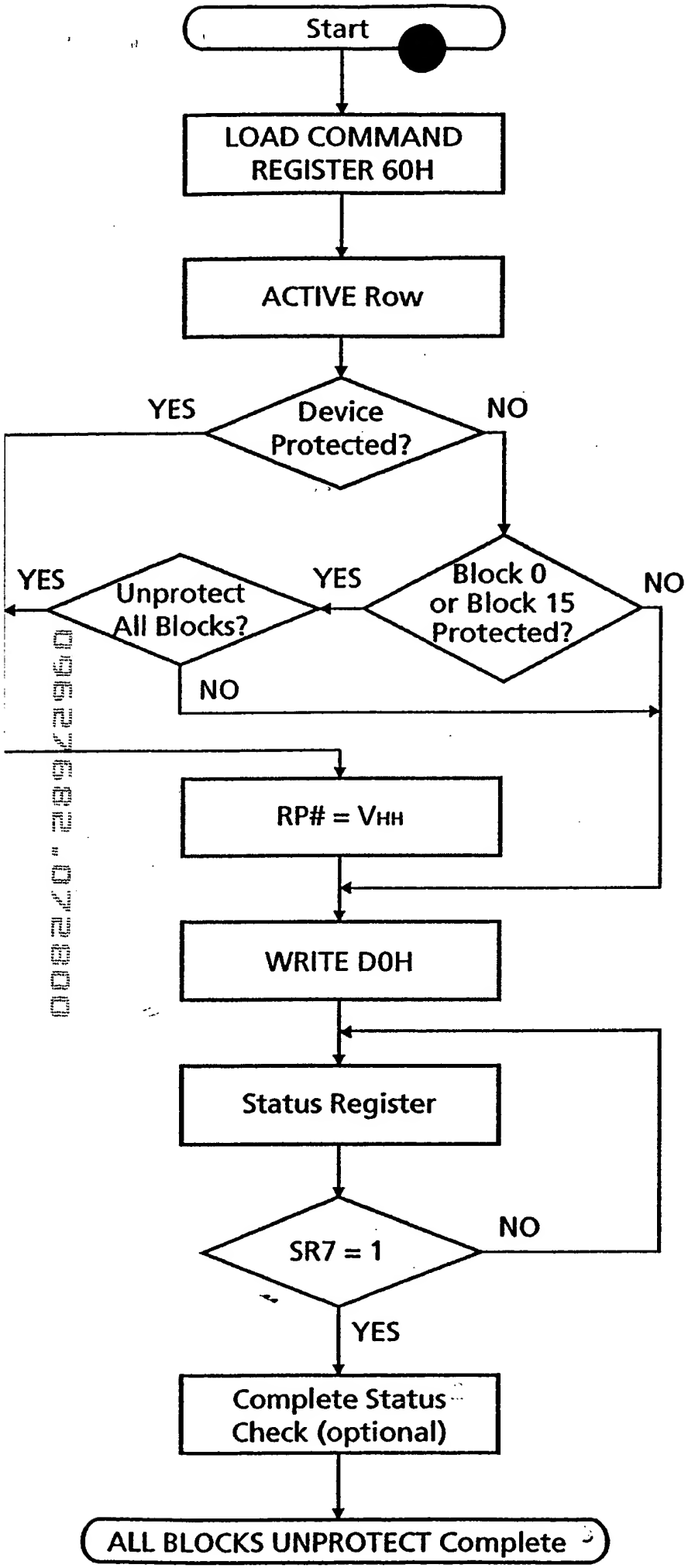

Start
LOAD COMMAND REGISTER 60H
ACTIVE Row
Device Protected?
YES
NO
Block 0 or Block 15 Protected?
YES
NO
Unprotect All Blocks?
YES
NO
RP# = VHH
WRITE D0H
Status Register
SR7 = 1
NO
YES
Complete Status Check (optional)
ALL BLOCKS UNPROTECT Complete

Fig. 23

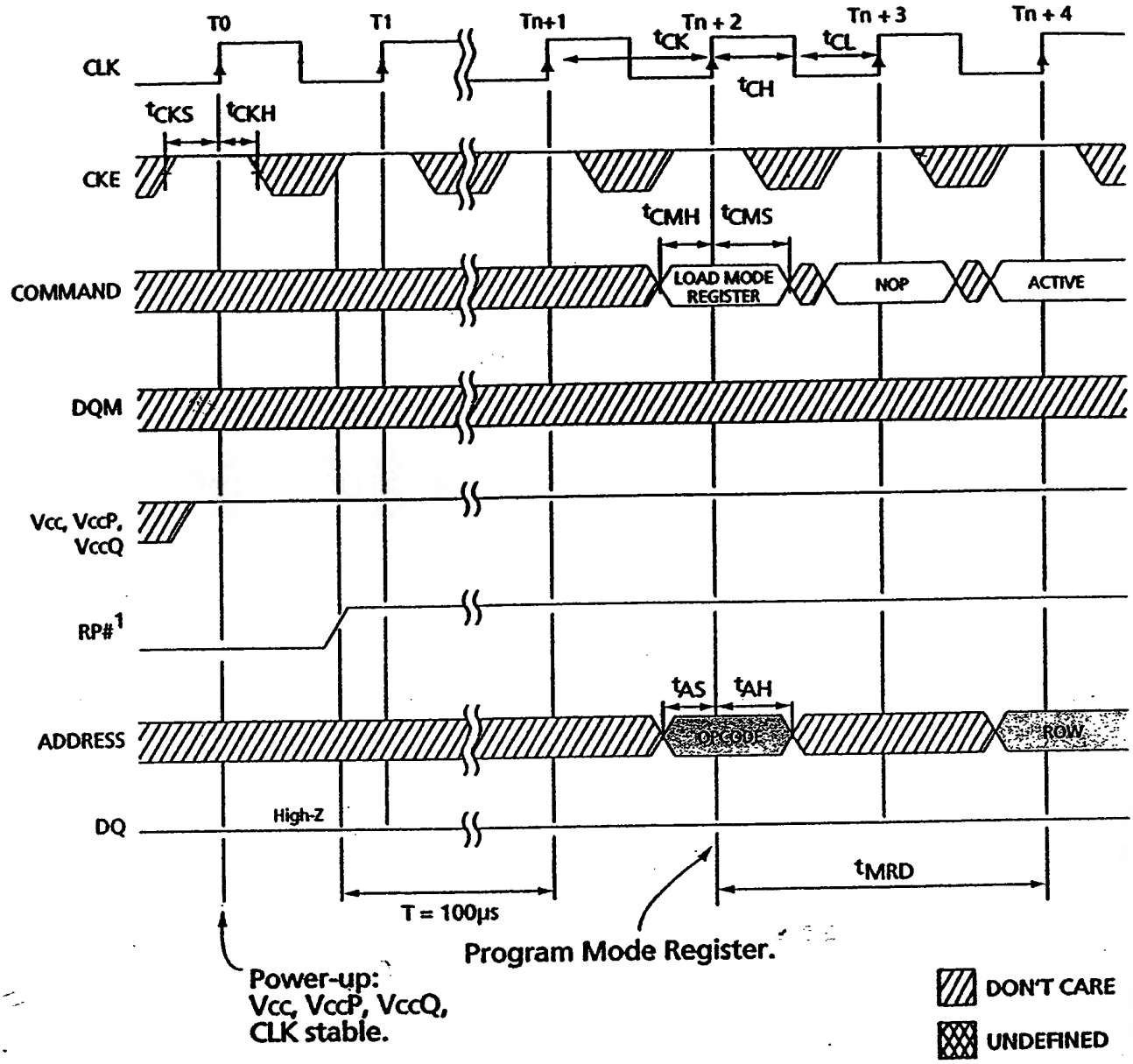

T0
T1
Tn+1
Tn + 2
Tn + 3
Tn + 4
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMH
tCMS
COMMAND
LOAD MODE REGISTER
NOP
ACTIVE
DQM
Vcc, VccP, VccQ
RP#1
tAS
tAH
ADDRESS
OP CODE
ROW
DQ
High-Z
tMRD
T = 100µs
Program Mode Register.
Power-up:
Vcc, VccP, VccQ,
CLK stable.
DON'T CARE
UNDEFINED

Fig. 24

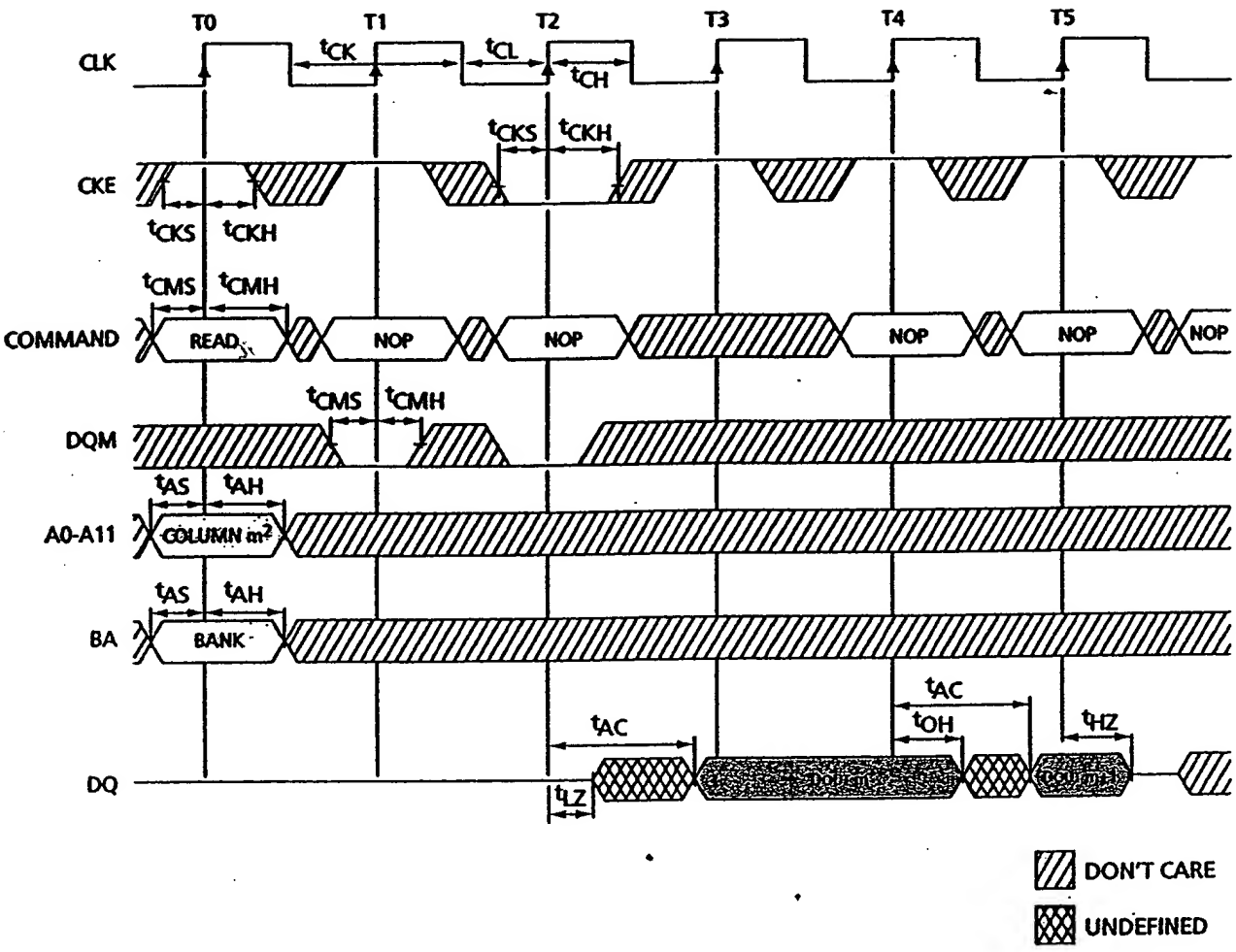

T0
T1
T2
T3
T4
T5
CLK
tCK
tCL
tCH
CKE
tCKS
tCKH
tCMS
tCMH
COMMAND
READ
NOP
NOP
NOP
NOP
NOP
DQM
tAS
tAH
A0-A11
COLUMN m
BA
BANK
tAC
tOH
tHZ
tLZ
DQ
DON'T CARE
UNDEFINED

Fig. 25

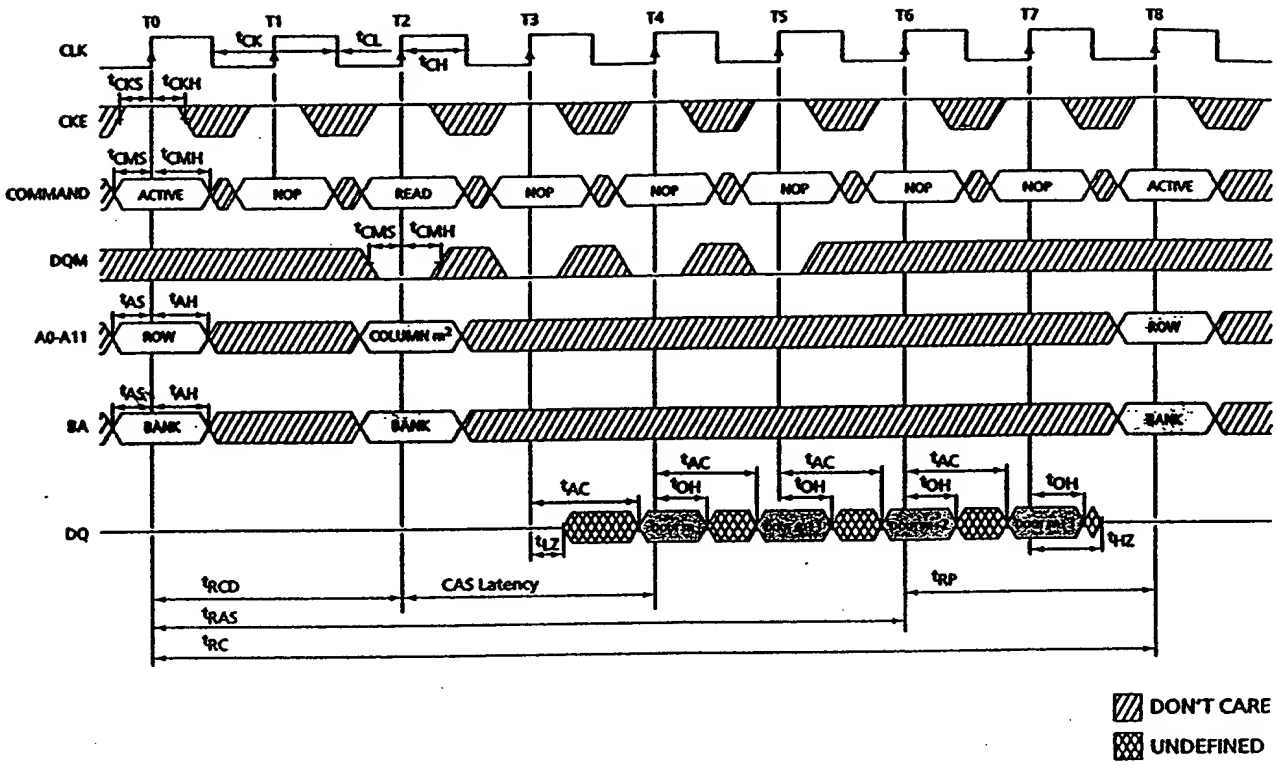

T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
CKE
COMMAND
DQM
A0-A11
BA
DQ
ACTIVE
NOP
READ
ROW
COLUMN m
BANK
tCK
tCL
tCH
tCKS
tCKH
tCMS
tCMH
tAS
tAH
tAC
tOH
tLZ
tHZ
tRCD
CAS Latency
tRAS
tRC
tRP
DON'T CARE
UNDEFINED

Fig. 26

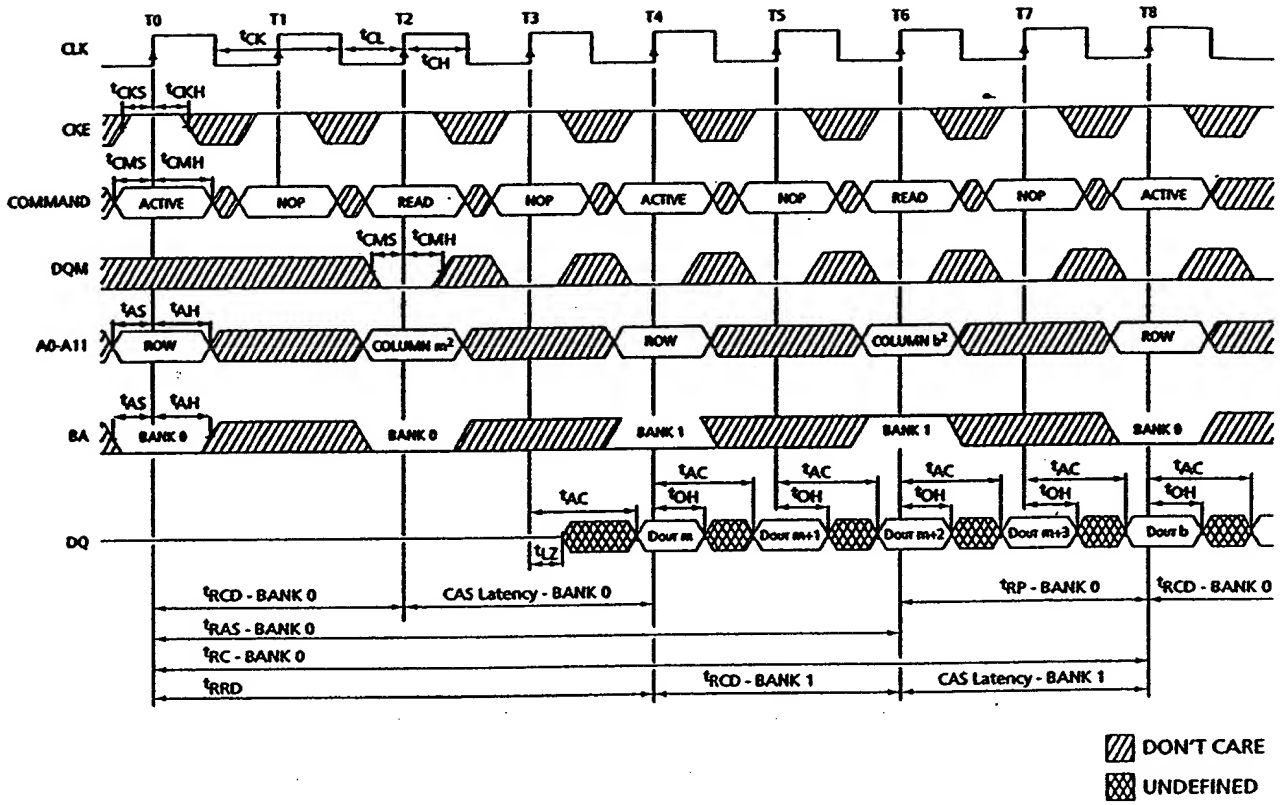


Fig. 27

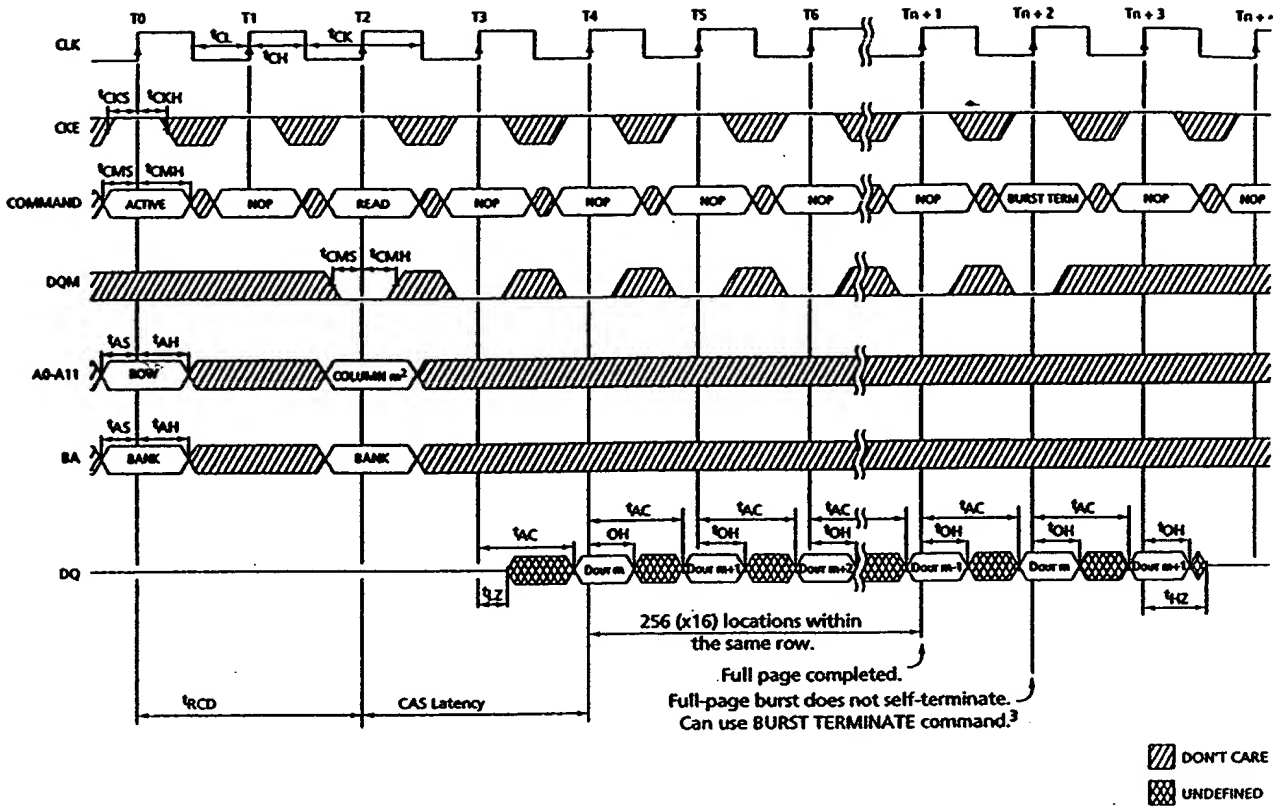

T0
T1
T2
T3
T4
T5
T6
Tn + 1
Tn + 2
Tn + 3
CLK
CKE
COMMAND
ACTIVE
NOP
READ
BURST TERM
DQM
A0-A11
BA
BANK
DQ
256 (x16) locations within the same row.
Full page completed.
Full-page burst does not self-terminate.
Can use BURST TERMINATE command.3
tRCD
CAS Latency
DON'T CARE
UNDEFINED

Fig. 28

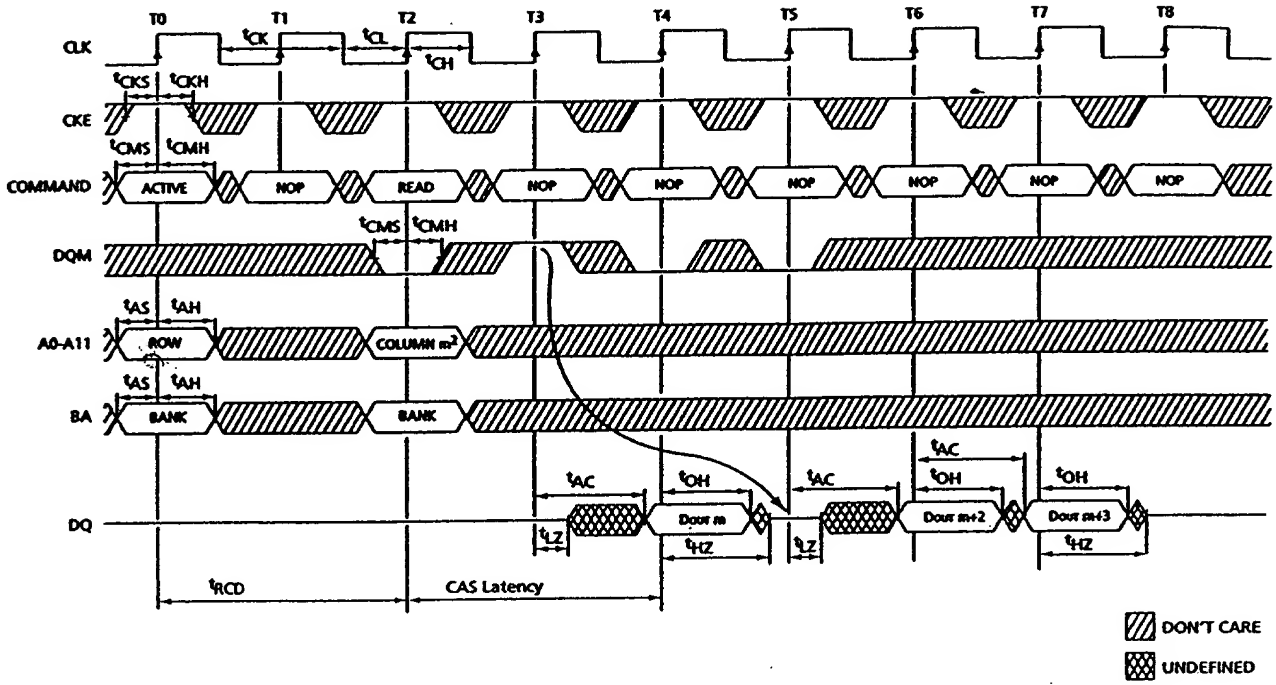


Fig. 29

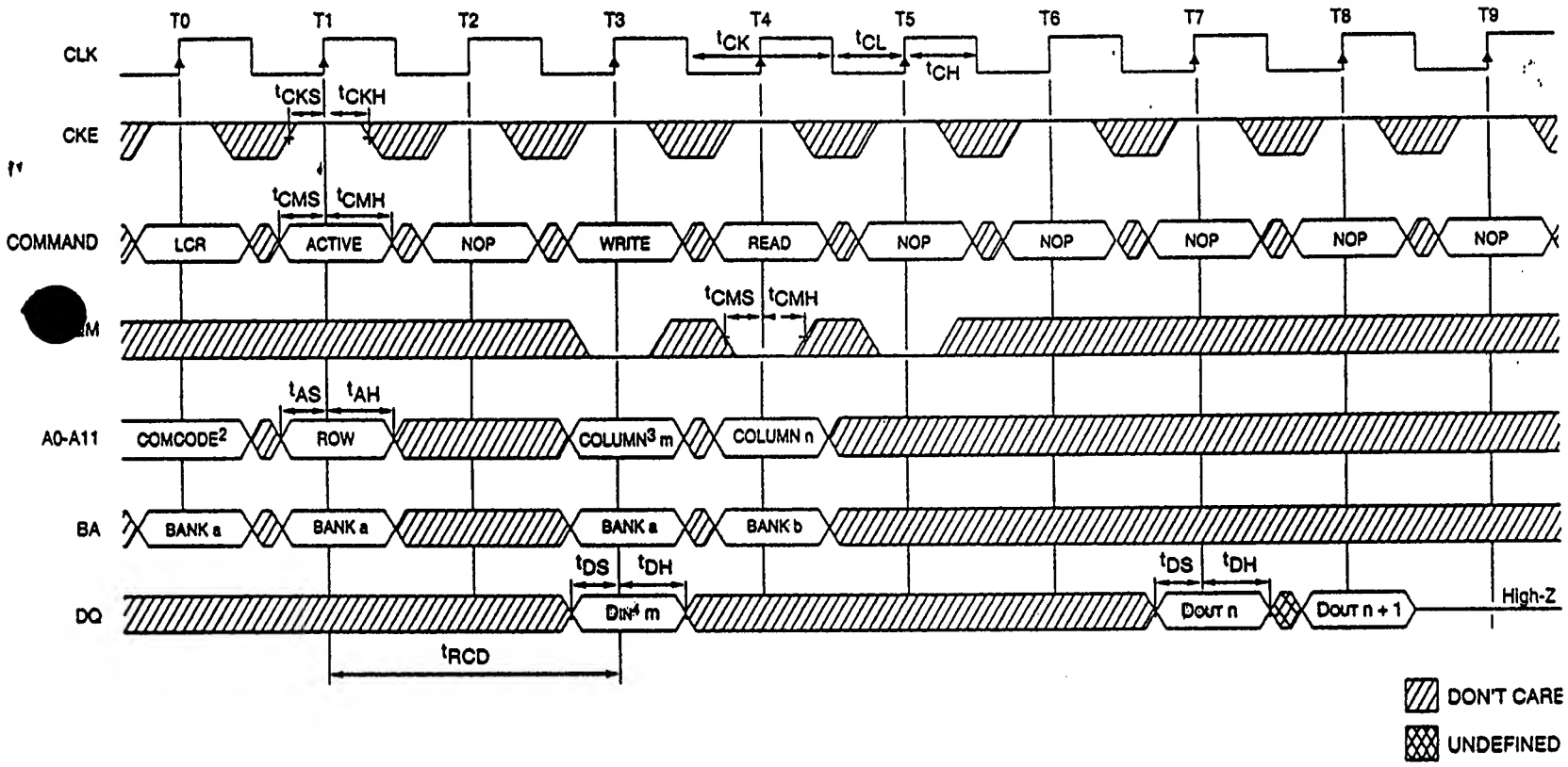

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
CLK
CKE
COMMAND
A0-A11
BA
DQ
tCK
tCL
tCH
tCKS
tCKH
tCMS
tCMH
tAS
tAH
tDS
tDH
tRCD
LCR
ACTIVE
NOP
WRITE
READ
COMCODE2
ROW
COLUMN3 m
COLUMN n
BANK a
BANK b
DIN4 m
DOUT n
DOUT n + 1
High-Z
DON'T CARE
UNDEFINED

Fig. 30

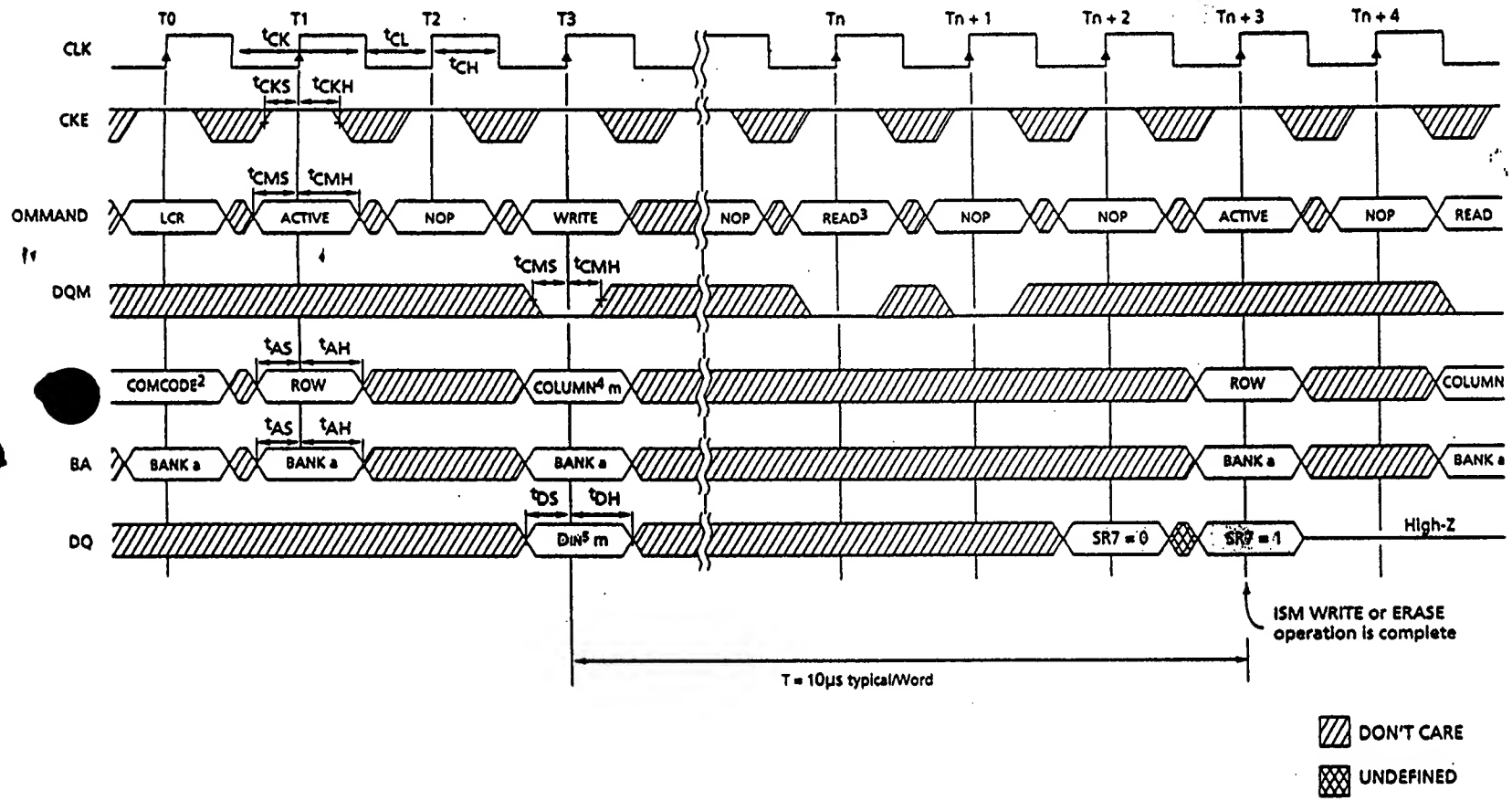

T0
T1
T2
T3
Tn
Tn + 1
Tn + 2
Tn + 3
Tn + 4
CLK
CKE
OMMAND
DQM
BA
DQ
tCK
tCL
tCH
tCKS
tCKH
tCMS
tCMH
tAS
tAH
tDS
tDH
LCR
ACTIVE
NOP
WRITE
READ3
READ
COMCODE2
ROW
COLUMN4 m
COLUMN
BANK a
DIN5 m
SR7 = 0
SR7 = 1
High-Z
ISM WRITE or ERASE operation is complete
T = 10µs typical/Word
DON'T CARE
UNDEFINED

Fig. 31

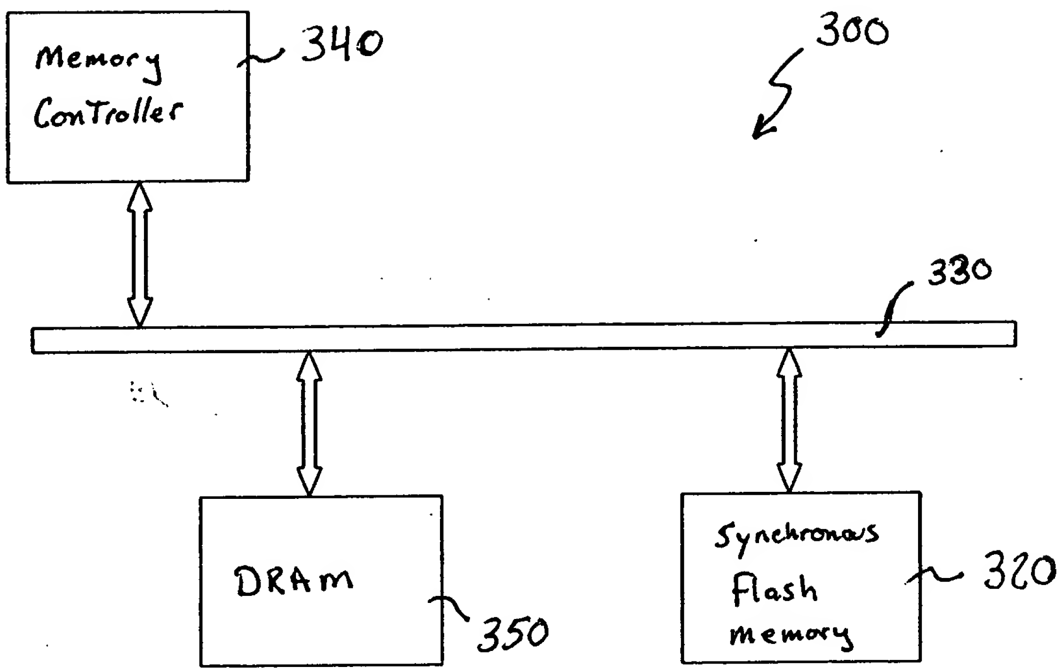


Fig. 32